LATS2019

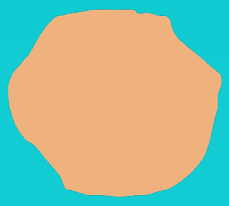
20th IEEE Latin-American Test Symposium
Santiago, Chile, 11th - 13th March 2019

PRELIMINARY CALL FOR PAPERS

www.lats.tttc-events.org

LATS2019

20th IEEE Latin-American Test Symposium
Santiago, Chile, 11th - 13th March 2019



CALL FOR PAPERS

The IEEE Latin-American Test Symposium (LATS, previously Latin-American Test Workshop - LATW) is a recognized forum for test and fault tolerance professionals and technologists from all over the world, in particular from Latin America, to present and discuss various aspects of system, board, and component testing and fault-tolerance with design, manufacturing and field considerations in mind. Presented papers are also published in the IEEE Xplore Digital Library. The best papers of the 20th LATS will be invited to re-submit to IEEE Design & Test,Journal of Electronic Testing: Theory and Applications - JETTA (Springer), Journal of Low Power Electronics - JOLPE (American Scientific Publishers), and IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD).

Topics of interest include but are not limited to:

- Analog Mixed Signal Test
- Automatic Test Generation
- Built-In Self-Test
- Defect-Based Test
- Design and Synthesis for Testability
- Design for Electromagnetic Compatibility
- Design for Reliable Embedded Software
- Design Verification / Validation
- Economics of Test
- Fault Analysis and Diagnosis
- Fault Modeling and Simulation
- Fault-Tolerance in HW/SW
- Fault-Tolerant Architectures
- Memory Test and Repair
- On-Line Testing
- Process Control & Measurements
- Radiation / EMI
- Hardening Techniques
- Software Fault-Tolerance
- Software On-Line Testing
- System-on-Chip Test
- Test Resource Partitioning
- Yield Optimization
- Hardware Security

Paper Submission Information:

To encourage and facilitate discussions, participation will be limited. Those interested in presenting recent results at the symposium are invited to submit an extended abstract, one to three pages long, or a full length paper. PDF electronic submissions must be done via the symposium's webpage: *www.lats.tttc-events.org*

Authors should send papers in the IEEE format. Detailed instructions are available at the symposium's webpage. The Program Committee also welcomes proposals for panels and special topic sessions.

For additional information, please contact the Program Chair:

Victor Champac – INAOE, Mexico
champac@inaoep.mx

Marcelo Lubaszewski, UFRGS, Brazil
luba@ece.ufrgs.br

Submission Deadline (Title and Abstract): November 9th, 2018
Submission (Full paper): November 16th, 2018
Notification of Acceptance: December 20th, 2018
Camera Ready: January 10th, 2019.

Santiago, besides many museums, theaters, restaurants, bars, houses a wide range of additional entertainment and cultural opportunities Its central location additionally makes it a great base for visiting surrounding cities and natural sites. Chile's steady economic growth has transformed Santiago into a modern Latin-American metropolitan area; with extensive suburban development, dozens of shopping centers, and impressive high-rise architecture, also counting with modern transportation infrastructure, including its steadily-growing Metro. Further, many multinational corporations have chosen the city for their regional headquarters.
All the above results in Santiago being the financial, cultural and political center of Chile and all positive aspects are bound by one integrational element: the kindness of its people.

Technical Sponsors:

The Institute of Electrical and Electronics Engineering, Inc.

tttc Test Technology Technical Council

IEEE Computer Society

Organized by:

TIMA Laboratory, France

Pontifical Catholic University of Chile

Financial Sponsors:

CEDA IEEE Council on Electronic Design Automation

Corporate Support:

SYNOPSYS